What is claimed is:

1. A non-volatile memory device comprising:

a memory gate pattern and a selection gate pattern separated from each other and arranged on a semiconductor substrate, the memory gate pattern comprising:

a tunnel dielectric layer, a floating gate, a first inter-gate dielectric and a control gate electrode, which are sequentially stacked,

the selection gate pattern comprising a gate dielectric layer, a bottom gate pattern, a second inter-gate dielectric and a top gate pattern, which are sequentially stacked,

wherein the width of the second inter-gate dielectric is narrower than the width of the bottom gate pattern.

2. The non-volatile memory device of claim 1,

wherein the second inter-gate dielectric extends from one sidewall of the selection gate pattern to approximately center thereof.

3. The non-volatile memory device of claim 1, wherein the control gate pattern and the top gate pattern further include a mask conductive layer, and wherein the mask conductive layer is formed on the first and second inter-gate dielectrics.

4. The non-volatile memory device of claim 1, wherein the top gate pattern is electrically connected to the bottom gate pattern.

5. A non-volatile memory device comprising:

a device isolation layer disposed on a semiconductor substrate to define a plurality of active regions;

selection lines extending across the active regions, the selection lines each including a bottom gate pattern, a second inter-gate dielectric and a top gate pattern, which are sequentially stacked; and

a plurality of word lines disposed between the selection lines to extend across the active regions and including a floating gate pattern, a first inter-gate dielectric and a control gate electrode, which are sequentially stacked,

wherein the width of the second inter-gate dielectric is narrower than the width of each selection line.

6. The non-volatile memory device of claim 5, wherein the second inter-gate dielectric extends from the one sidewall of the selection line to approximately center of the selection line.

7. The non-volatile memory device of claim 5, wherein the floating gate pattern is interposed between each of the active regions and the word line, and wherein the bottom gate pattern is disposed under the top gate pattern to extend across the active regions.

8. The non-volatile memory device of claim 5, wherein the second inter-gate dielectric crosses over the active regions.

9. The non-volatile memory device of claim 5, further comprising:

a mask conductive layer disposed between the second inter-gate dielectric and the top gate pattern; and between the first inter-gate dielectric and the control gate electrode.

10. The non-volatile memory device of claim 5, wherein the first and second inter-gate dielectrics include at least a single dielectric layer having a dielectric constant higher than that of a silicon oxide layer.

11. The non-volatile memory device of claim 5, further comprising:

a second active region defined by the device isolation layer; and

a peripheral gate pattern crossing over the second active region,

wherein the peripheral gate pattern includes a bottom conductive pattern and a top conductive pattern sequentially stacked to be electrically connected to each other.

12. A method for fabricating a non-volatile memory device, the method comprising:

forming a device isolation layer on a semiconductor substrate to define a plurality of active regions;

forming a first conductive layer on the plurality of active regions;

patterning the first conductive layer to form a first conductive pattern on the active regions;

forming an insulating layer on the first conductive pattern;

patterning the insulating layer to form an opening extending therethrough, the opening exposing a portion of the first conductive pattern;

forming a second conductive layer on the patterned insulating layer and on the exposed portion of the first conductive pattern through the opening; and

sequentially patterning the second conductive layer, the patterned insulating layer and the first conductive pattern to form a bottom gate pattern, an inter-gate dielectric, and a top gate pattern, wherein the width of the inter-gate dielectric is narrower than the width of the bottom gate pattern.

13. The fabricating a non-volatile memory device of claim 12, wherein the gate pattern is partially overlapped with the opening to extend across the active regions, the gate pattern extending in parallel to the opening.

14. The fabricating a non-volatile memory device of claim 12,

wherein the second inter-gate dielectric extends from one sidewall of the selection gate pattern to approximately center thereof.

15. The fabricating a non-volatile memory device of claim 12, wherein the top gate pattern is electrically connected to the bottom gate pattern.

16. The method for fabricating a non-volatile memory device of claim 12, further comprising forming a mask conductive layer on the insulating layer, wherein the opening is formed by sequentially patterning the mask conductive layer and the insulating layer.

17. The method for fabricating a non-volatile memory device of claim 16, wherein sequentially patterning the second conductive layer, the patterned insulating layer, and the first conductive pattern comprises:

patterning the first conductive pattern, using the insulating layer as an etch stopping layer, to form a control gate electrode and the top gate pattern; and

pattering the insulating layer and the first conductive pattern to form a floating gate and the bottom gate pattern.

18. The method for fabricating a non-volatile memory device of claim 16, wherein the floating gate and the bottom gate pattern align with the control gate electrode and the top gate pattern, respectively.

19. A method for fabricating a non-volatile memory device, the method comprising:

forming a device isolation layer on a semiconductor substrate to define a cell region and a peripheral region and to define a plurality of first active regions in the cell region and a second active region in the peripheral region;

forming a first conductive layer on the semiconductor substrate;

patterning the first conductive layer in the cell region to form a first conductive pattern on the first active regions;

forming an insulating layer on the first conductive pattern;

patterning the insulating layer to form an opening crossing over the first active regions, while exposing a portion of the first conductive layer in the peripheral region;

forming a second conductive layer overlying the insulating layer; and

sequentially patterning the second conductive layer, the insulating layer and the first conductive pattern to form a word line, a selection line and a peripheral circuit gate pattern,

wherein the word line crosses over the first active regions, and

wherein the selection line is partially overlapped with the opening to extend across the first active region, the selection line extending in parallel to the opening, and

wherein the peripheral circuit gate pattern crosses over the second active region.

20. A non-volatile memory device comprising:

a semiconductor substrate;

a gate line formed on the substrate, the gate line including:

a gate dielectric layer, a bottom gate pattern, an inter-gate dielectric and a top gate pattern, which are sequentially stacked on the substrate,

wherein the width of the inter-gate dielectric is narrower than the width of the bottom gate pattern.